Network-on-Multi-Chip (NoMC) with monitoring and debugging support

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Abstract — This paper summarizes recent research on Network-on-Multi-Chip at Poznan University of Technology. The proposed network architecture supports hierarchical addressing and multicast transition mode. Such an approach provides new debugging functionality hardly attainable in classical hardware testing methodology. A multicast transmission also enables real-time packet monitoring. The introduced features of NoC network allow to elaborate a model of hardware video codec that utilizes distributed processing on many FPGAs. Final performance of the designed network was assessed using a model of AVC[4] coder and multi-FPGA platforms [12][13]. In such a system, the introduced multicast transmission mode yields overall gain of bandwidth up to 30%. Moreover, synthesis results show that the basic network components designed in Verilog language are suitable and easily synthesizable for FPGA devices.

Keywords — debugging, FPGA, multi-chip, NoC, video coding,

1. Introduction

Network-on-Chip (NoC) is a relatively new design approach that provides a methodology of implementing Systems on Chip (SoC) interconnections. NoC-based systems incorporate a network infrastructure that offers remarkable improvement over conventional communication systems like bus-based or circuits-switching-based [1]. Because basic network components are reused, there is no need to implement network infrastructure from the scratch and thus, the design costs related to communications are reduced. Moreover, scalability of the system is greatly improved because new devices can be added in a structured way. Finally, NoCs provide communication abstraction, which allows independent design of devices [2]. NoC based architecture can be used in both ASICs and FPGAs. Commonly, the first step of system design is to implement the system on FPGAs and the second is to move it to ASIC [3]. In most of cases, the circuit optimized for FPGA is also efficient as ASIC (but not in reverse). Due to this fact, it is more worthy to consider NoC networks for FPGAs. In order to create a useful and efficient NoC architecture, the proposed solutions should meet certain requirements related to transmission bandwidth, communication latency, structure flexibility and many others. The implementation cost and possibility to reuse NoC component is also important. In practice, when complex hardware is designed (such as a video encoder) certain features such as scalability and unified communication interfaces are highly expected.

Hardware implementations of recent video coding standards, as for example Advanced Video Coding AVC/H.264 [4], consist of many compression tools and pre-/post-processing blocks. Additionally, in order to implement a decoder or encoder that works in real time parallel processing has to be applied. It means that the design consists of many processing elements that require high communication bandwidth (especially with memory) and in some cases the whole design requires more than one device (FPGA).

The work has been aimed at development of a communication infrastructure based on the idea of Network-on-Chip, which allows to dynamically combine multiple integrated circuits and will support the testing and monitoring functionalities, as a result, a new variant of Network-on-Chip have been proposed. The new network architecture will have none of the drawbacks listed in the section below.

2. Main Network-on-Chip drawbacks

As it was already said, Network-on-Chip (NoC) is an efficient solution for connecting modules of hardware application but has two main drawbacks:

i) There is **no scalability and flexibility** for multi-chip systems. Scalability may be achieved by using a hierarchy in interconnect system. However, not all hierarchical networks are flexibly scalable in terms of multi-chip scalability. Some works, e.g. [5][6], introduce a hierarchy to improve flow of network traffic and ease resource management but the proposed NoC extensions are not suitable for multichip systems because any change in the structure of the network requires its reconstruction. Another example has been shown in [7]. Despite it is designed for hierarchical arrangement of Chip-Multi-Processors (CMP), based on mesh topology, such structure is inefficient in the case of non-homogeneous tiles. Moreover, mesh topology, as a higher level interconnect system, is hardly scalable. There are more solutions [8][9] but none of them is appropriate, nor do they meet the aforementioned requirements.

ii) **Only a unicast transmission is supported** but in multimedia applications, as for example video encoding, many processing cores use the same source data. In the case of the unicast transmission these data need to be sent to their destinations multiple times. Such unnecessary data transmissions can be significantly reduced by applying the multicast transmission.

3. Network-on-Multi-Chip

The authors propose a variation of NoC for multi-chip systems called Network-on-Multi-Chip (NoMC). The NoMC is a **hierarchical NoC network**. The proposed way of intergroup and interchip connection management enables dynamic linking of multiple chips without a need of redesigning. In general, the NoC structure has been split into two areas: local and global. The global part of NoC has a tree structure with full dynamic of the linking mechanism, but the local one can be implemented as any structure with one gateway to the global part. This solution simplifies system expansion with new functionalities/processing cores.
Additionally, to provide efficient data processing and to improve network performance authors introduce **a multicast transmission**. The idea is simple: more than one destination address in packet header is allowed (Fig.3). Although, the implementation requires proper packet replication in network switches, we get ability to send the same data to several locations, even to several chips. Moreover, because it is possible to add an additional address to any packet, we suddenly get the ability to send all packets not only to primary destination location but also to debag/monitoring location. In this way the authors achieve very useful additional functionality on the NoC level that is not yet described in literature.

4. Scalability and hierarchical addressing

We consider scalability in terms of the ability to easy extend the system by new hardware components. Our new scalable architecture of NoMC consists of 3 levels of hierarchy, starting from the lowest level:

- **Local network** - also called a **group** of processing elements (PEs), that contains PEs, network interfaces called EndPoints (EPs) and routers. One chip consists of at least one group of PEs.
- **Cluster level** that provides connectivity for a set of groups (local networks) (Fig. 1a). One chip can consist of more than one cluster, but for small projects only a local network may exist without higher level of hierarchy.
- **System level**, which is introduced to interconnect clusters. The higher level of interconnects enables linking multichip boards together. Active elements at the system level are characterized by hot plug support.

We also introduce gateways to the NoC network, which separate all of the hierarchy levels from each other. The main goal of gateways is to parse packets and extract or include information necessary for proper routing. Such an approach allows designing of each hierarchy level individually. The local network architecture is defined with only a set of devices (routers and EndPoints i.e. network interfaces for PE) that can be connected applying any topology. Since routers are expensive in terms of hardware consumption, their number should be as low as possible. In comparison to commonly known network interfaces [10] the functionality of EndPoint has been extended to meet the aforementioned requirements. The EndPoints are able to perform basic switch-

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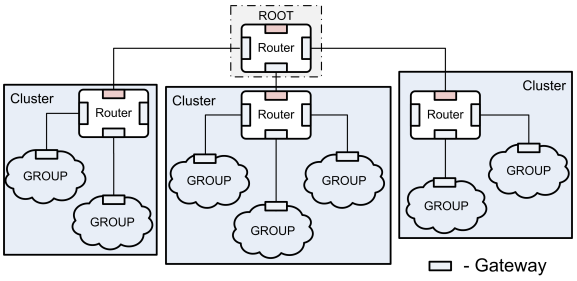

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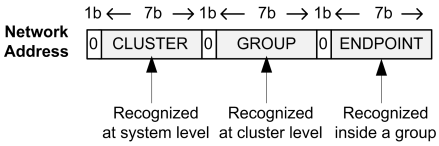

Fig. 1. a) Hierarchical structure of cluster and system level of a network, b) network address format.

ing operations and may be connected to each other without a need for more sophisticated routers. The detailed description of the hierarchical addressing was presented in previous works [12-17]. The addressing scheme is adjusted to hierarchical architecture (Fig. 1b). Each address consists of three parts, each referring to one level of network hierarchy. At a particular level only own part of address is recognized. In order to introduce multicast transmission mode the authors propose to add more than one destination address per packet (Fig 3), each address is then checked in every network element (gateways, routers, etc.). The packet is copied if routes for any of the destination addresses are splitting. The proposed solution for external network architecture (cluster and system level) is based on a tree topology. Distinction between cluster and system level has been introduced in order to connect clusters flexibly. Moreover, tree structure allows designing of a simplified routing algorithm and packet handling protocol which yield reduction of hardware consumption.

5. Multicast transmission

Classical NoC networks support only simulcast transmission, which is enough for most simple applications, but is not sufficient for complex applications and for debug and monitoring features. Our research indicated that implementation of multicast (similar mode to the Ethernet Network) is possible: instead of a single destination address, multiple addresses are assigned to every packet (Fig.2). The main change includes network routers which must be able to duplicate packets consisting multiple addresses. This

means that the main cost of multicast feature implementation is placed in routers. As it has been already said, multicast functionality allows sending of a copy of the packet to any location but in a particular case it may be a monitoring/debugging device. In order to design a router that uses

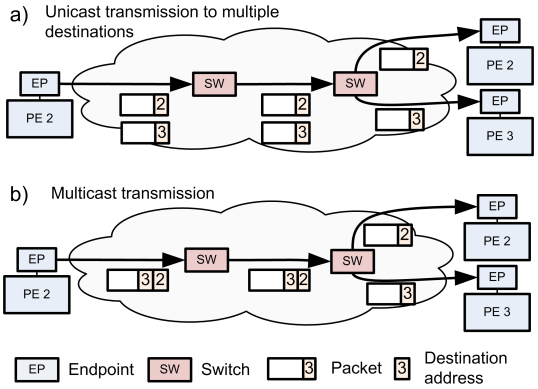

Fig. 2. Unicast/Multicast communication with example of packet replication.

a reasonable amount of memory, the network packets size has been limited to 32 words. Such short packets/messages make network traffic more fluent and reduces the cost of packet replication process. Packets always start with the field *D*estination Address and end with *E*ndOfPacket command, as shown in Fig. 3.

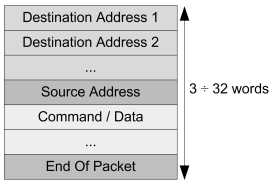

Fig. 3. NoMC packet structure with multiple destination address.

6. Debugging and monitoring features

As a result of introducing of the multicast feature we have obtained additional functionality such as debugging and monitoring. The well-known standard for in-circuit test is JTAG [4] protocol, which is intended for system management tasks. It requires two physical components: test access port (TAP) which interprets JTAG protocol, and boundary scan register (BSR). Implementing of those modules in each PE may require large amount of chips resources regarding the scale of current designs. There are several approaches in literature of NoC embeded debugging functionality [5-9], but the hardware cost of this functionality is still significant. Moreover, the described proposals are not scalable and mostly based on JTAG standard. None of them offers full and scalable monitoring feature [13][18]. Multicast based mechanism introduced by the authors include real-time monitoring, management of the devices and system configuration. The debugging is supervised by the so-called Remote Debugging Host (RDH) (Fig.4). RDH is an off-chip control device or software application on a personal computer, connected to the system with any physical interface. The role of RDH is to provide user interface to the debugging functionality, such as: applying test vectors, gathering debugging data, handling exceptions or emulating hardware devices in software. More about multicast transmittion and debugging can be found in [12-17].

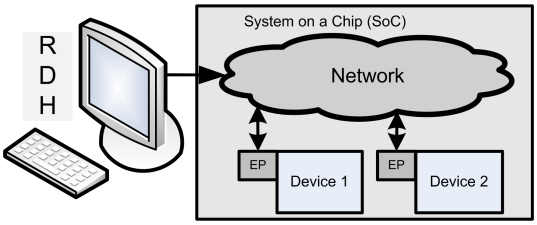

Fig. 4. System with one RemoteDebugHost (RDH) as a root and examoplary System-on-Chip.

Debug-mode in the EndPoint forces sending of a copy of each packets outgoing to RDH. Endpoints use multicast transmissions and add RDH address to the packets address list. Debug-mode can be switched on and off for each endpoint individually. RDH receives packet duplicates and with the use of specific application is able to recognize and present packets data to the user. Also, correctness of packets and data format can be verified. With sufficient network bandwidth, real-time debugging/monitoring is possible.

The authors have assessed the proposed ideas during design, implementation and testing process of AVC/H.264 video decoder (Fig.5). At that time, many examples of debugging functionality usage were observed, which otherwise would be very difficult to attain. For example, without debugging functionality, it would be required to resynthesize the whole project with additional testing benches in order to test what was wrong: the transmission through the link was corrupted, there was some kind of hazard situation somewhere or it was just a synthesis error.

7. Hardware Platform

In order to verify the proposed solutions a hardware platform has been designed and produced. The test platform made at Poznan University of Technology consists of 2 to 9 FPGA devices. A Xilinx FPGA Virtex-4/5 and Spartan-3 devices have been used (Fig.5,7). All the NoMC network components were implemented in Verilog hardware description language and synthesized using the ISE design suite. Using such a system, the authors were able to conduct many experiments for various NoMC configurations and for a wide range of parameters.

In Table 1 the synthesis results of basic network components are shown. As one may see, for 32-bit bus of NoC and Spartan-6 FPGA, it is possible to achieve 1GB/s of throughput.

Table 1
Synthesis results for Spartan6 XC6SLX75-3 FPGA device.

Elements	LUT	FlipFlop	CLK (MHz)
Router (4 ports)	1106 (2%)	759 (1%)	278.8
Router (3 ports)	647 (1%)	573 (1%)	277.3
EndPoint	436 (1%)	345 (1%)	315.4
Gateway	515 (1%)	409 (1%)	315.3

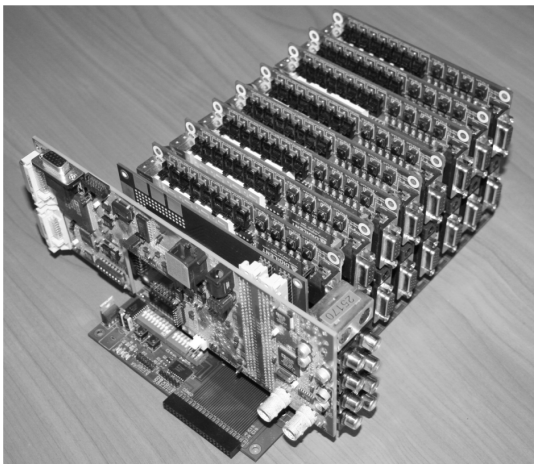

Fig. 5. The Multi-board experimental system with FPGA devices and an SDI video grabber.

8. Conclusions

In this paper, the authors summarize research and development of new NoMC architecture. In the course of development of addressing scheme and packet flow control in the network strong emphasis was put on certain features, such as multichip scalability, debugging and monitoring functionality that was expected. Consequently, the new architecture of interconnect system consists of three levels of hierarchy, each separated with a dedicated device, referenced as a gateway. As it was highly expected, the multicast transmission mode which provided improved network performance and significant reduction of the required bandwidth was successfully introduced.

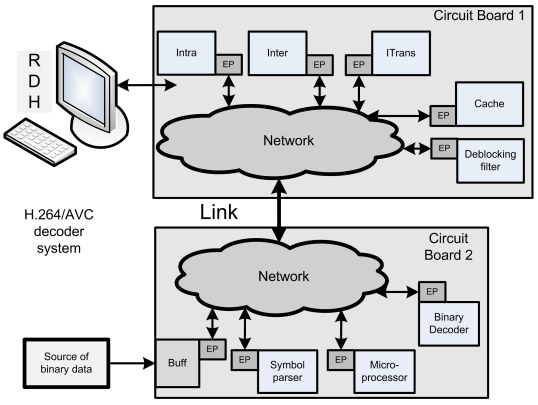

Fig. 6. The implemented H.264/AVC system on two circuit boards with RemoteDebugHost and external source of testing data.

The main achievements include expansion of network to support the packet remote monitoring and hierarchical addressing for scalability support. An assessment of the proposed debug system on an exemplary real debugging scenario has been made using multi-FPGA boards (Fig. 6,7).The authors tested many applications targeted to distributed systems. Among them a AVC/H.264 decoder, motion estimation algorithm and several transmission and data broadcast schemes (for example realtime HD video sequence capture and video data broadcast to all FPGA devices in system (Fig.7)). Finally, the conducted research and analysis prove that the designed Network-on-Multi-Chip works correctly and meets all the assumed requirements.

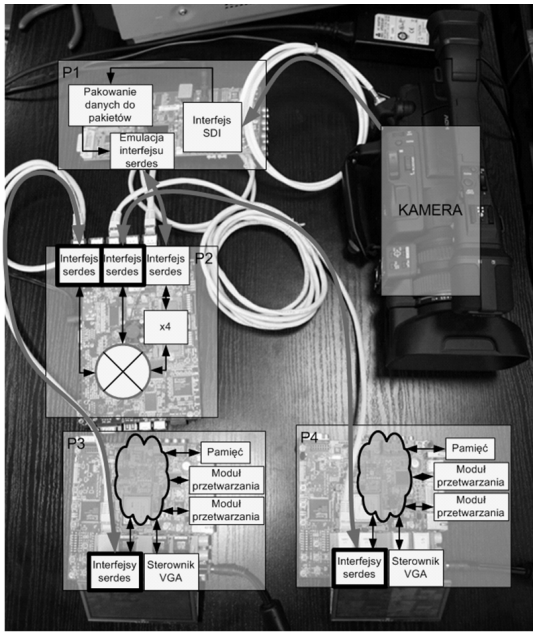

Fig. 7. A video capture and processing system based on two Virtex-4 boards with a video grabber.

9. Acknowledgements

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